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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,160	10/04/2000	James Daniel Merchant	CYPR-CD00055.US.P	1666

7590 02/14/2003

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EXAMINER
HAMILTON, MONPLAISIR G

ART UNIT	PAPER NUMBER
2172	

DATE MAILED: 02/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,160	MERCHANT ET AL.	
	Examiner	Art Unit	
	Monplaisir G Hamilton	2172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *17 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 are pending. The communication filed on 12/17/02 amended Claims 5, 6, 8, 17, and 18. Claims 1-20 remain for examination.

Drawings

2. The proposed drawing correction, filed on 12/17/02 has been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Response to Arguments

3. Applicant's arguments filed 12/17/02 have been fully considered but they are not persuasive.

Applicants specifically argue that Mason:

"fails to disclose or suggest identifying a plurality of memory cells in a hierarchical schematic representation of a programmable device....Moreover, Mason actually teaches away from the limitation of identifying a plurality of memory cells in a hierarchical schematic representation of a programmable device. Mason at col. 2 lines 57-62 and Figure 1 discloses a coordinate system to identify the location of logic cells. The cells are numbered left to right and from top to bottom in an array-like fashion, as opposed to a hierarchical fashion...Mason fails to disclose or suggest automatically storing a plurality of logical names for a plurality of memory cells in a hierarchical schematic representation of a programmable device"

Examiner disagrees with applicant. Mason discloses the use of a design entry-module to create the initial design (col 6, lines 25-30). Mason further discloses a look-up table can be implemented as a cascaded series connection of 2-input AND gates and 2-input OR gates (col 10, lines 24-26). This implementation of the look-up table is a hierarchical representation of a programmable device. In addition to this disclosure of a hierarchical schema, Mason discloses cells can be grouped as sets of horizontal or vertical cells (col 8, lines 5-10), this is equivalent to the claimed hierarchical schema because it allows for "a ranked series" [Merriam-Webster's Collegiate Edition - Tenth Edition]. Furthermore Mason discloses "automatically storing said plurality of logical names for said plurality of memory cells within a data structure" (col 7, lines 12-18).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-7 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5946219 issued to Mason et al herein referred to as Mason.

Referring to Claims 1-7 and 14-20:

See Office Action mailed 9/12/2002.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5946219 issued to Mason et al herein referred to as Mason as applied to Claims 1-7 and 14-20 above, and further in view of US 5838583 issued to Varadarajan et al, herein referred to as Varadarajan.

Referring to Claim 8:

Referring to Claim 8:

Mason discloses a computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:

a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses (col 5, lines 14-16);

b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device (col 4, lines 39-42; col 10, lines 12-15);

c) ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); (col 10, lines 16-22)

Mason does not explicitly disclose the claimed "d) storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading data into a programmable logic device."

Varadarajan discloses d) storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading data into a programmable logic device (col 9, lines 28-40).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Mason to store logical names that describe the order of loading data into a programmable device. One of ordinary skill in the art would have been motivated to do this because it would allow the designer to control the logic follow in a datapath (Varadarajan col 9, lines 40-41). Also the design engineer can easily reconfigure the PLD without performing place and route operations (col 4, lines 53-58).

Referring to Claims 9-13:

See Office Action mailed 9/12/2002.

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6237129 issued to Patterson, Cameron D. et al. Patterson discloses a method whereby placement information for elements of a logic module is specified in such a manner that specific coordinates need not be included. This method can be applied to any module or other element having an associated placement in a programmable device. Using the method of the invention, relative coordinates (such as the RLOC constraints discussed in relation to the prior art) need not be specified. Instead, the invention introduces a vector-based form of layout.

US 5754441 issued to Tokunoh, Seiji et al. Tokunoh discloses an LSI automated design satisfying a required function and a required performance with the reuse of existing design data, there are disposed: library element memory means for storing, in the form of elements, existing design data (circuit data) together with design procedures (conversion information) thereof; element arrangement entering means for entering an element arrangement for achieving the desired function; library element specializing means for determining the functions of general-purpose elements.

Final Rejection

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monplaisir G Hamilton whose telephone number is 1703-305-5116. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on 1703-305-4393. The fax phone numbers for the organization where this application or proceeding is assigned are 1703-746-7239 for regular communications and 1703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 1703-305-3900.

Monplaisir Hamilton
February 4, 2003

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100